NMOS Transistor Design and Fabrication for S-Parameter Extraction

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Abstract— **A successful test layout for S-parameter analysis was demonstrated. Process characterization accomplished as part of this project demonstrated a pseudo-shallow trench isolation. Active device measurements would have been possible with a DC blocking fixture. 0.37μm-1.0μm transistors were fabricated with a non-ideal characteristic which was due to the source drain implant being blocked by oxide residue from the spacer formation etch.**

Index Terms—**submicron NMOS, S-parameter measurements.**

I. Introduction

In order to characterize transistor performance for analog circuit design, the frequency response of the devices must be taken into account. S-parameters are used to characterize transistor performance, as a function of frequency [1]. This technique treats a transistor as a two-port network, and measures the power transfer throughout the system being tested. This test has the advantage of being able to extract the parasitic capacitance, which impair transistor operation. S-parameter testing has restriction on the way that the devices may be laid out. The signals must be taken to the device in a ground/signal/ground configuration; this reduces the loss of signal due to incorporation of external noise. In the case of this design a dual polysilicon gate was used so that the source contacts, which are grounded for device testing, would isolate the gate signal as well as the signal being received from the drain. The test setup must also be calibrated for the noise already in the system. Special calibration structures are required for this, shorts, opens and through circuits. The shorted devices have the source, drain and gate contacts attached together. This allows for the resistance of the pads to be subtracted from subsequent active measurements. The open circuits eliminate the pad capacitance, and the through circuits eliminate the transmission line inductance. An NMOS transistor process was created keeping parasitic elimination the central design element.

This work is part of the senior design project requirement for a B.S. degree in Microelectronic Engineering at the Rochester Institute of Technology (RIT). The results of this project were presented at the 23rd Annual Microelectronic Engineering Conference on May 10, 2005 at RIT in Rochester, NY. Adam James is with the Microelectronic Engineering Department at the Rochester Institute of Technology.

II. Process and Device Design

The NMOS process that was developed had three major objectives, (i) the device was to be robust against process variations, (ii) the process was to be easily controlled with the tool set used, and (iii) the fabrication time length was to be kept to a minimum to ensure complete fabrication within the time allotted. The gate length geometries were determined from previous lithographic experience in the laboratory. The process from the previous work was not used, and a new process was developed. The new process was to include shallow trench isolation between devices, low-doped source drain extensions, and silicided contacts. The device was designed using Silvaco Athena. The NMOS fabrication process begins with a lithography step. The wafers were coated using the SMFL standard coat recipe, and exposed using the trench isolation mask. This mask is a dark field mask with openings that define the trench dimensions. The wafers were exposed on the Canon 1400i i-line stepper, with a dose of 160mj/cm^2. It was noted that the dose required for optimum exposure depended greatly on the humidity in the lithography bay. This dose dependence is due to the photoresist thickness, which on the coat track depends on humidity. If the humidity is low in the bay the dose will need to be increased. The optimum focus for this level was found to be -0.5μm. Once the wafers were developed on the SSI track, using the standard SMFL develop recipe, the wafers were baked on a manual hotplate at 140 ° C for 1 minute. This baked helped to establish a stronger etch resistance to dry etching, however the features are distorted by a slight 0.05 μm on each side reflow of the resist at this temperature. The trenches for isolation were then etched into the wafer by using an SF_6 dry etch in the Drytek Quad RIE etcher. In order to establish the chamber characteristics needed for a reproducible etch, the chamber was run with oxygen/argon plasma. The recipe used calls for a chamber pressure of 300 mTorr, an oxygen flow rate of 100 sccm, an Ar flow rate of 15 sccm, and a power setting of 185 watts. This five-minute clean was used to remove any polymeric build up from other users on the gas showerhead in the chamber. If non-reproducible results were obtained a physical cleaning of the chamber was performed using an alpha wipe, and isopropyl alcohol to remove build up on the gas showerhead. Care was taken not to scratch or damage the chamber anodization. The silicon etch was performed for 45 seconds for a 0.75 μm deep trench. The recipe used had an SF_6 flow rate of 70 sccms, a chamber pressure of 70mtorr and

a power setting of 185 watts. The results from this etch are shown in Fig. 1.

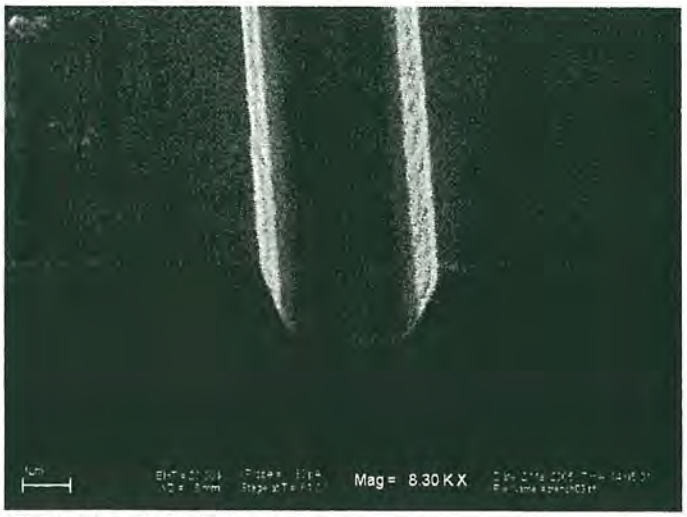

Fig. 1. Trench Isolation etch.

It can be seen from the SEM images that the edge of the etched profile is rough. This roughness was fixed by a thermal oxidation, but first the photoresist was removed from the wafer via an ashing oxygen plasma. The trench depth was varied from 0.75-2 μm. After ashing an RCA chemical clean was performed, this clean consists of three chemical stages, the first chemical stage is a mixture of HCl and Hydrogen Peroxide. This chemical bath removes any metallic components, which are present on the wafers surface. The wafers are rinsed in deionized water, which dilutes and rinses away the HCl mixture. The hydrogen peroxide acts to mediate the HCl so that it does not pit the wafer surface. The next chemical step is a 1-minute etch in 100:1 Hydrofluoric (HF) acid. This removes any native oxide that is on the wafer surface. The wafer is then rinsed, followed by an organic removal step, which is a chemical bath of ammonium hydroxide, and hydrogen peroxide. Following the RCA clean, 1000 Å of oxide was grown in dry oxygen ambient at 1000°C. The wafers were then etched in HF to remove the thermal oxide, and smooth out the etched sidewalls. The wafers were then reoxidized using the same process as above. The purpose of this thermal oxide was to act as a liner for following Tetraethylorthylsilicate (TEOS) depositions. The thermal oxide, which is grown rather than deposited, has much less charge, and traps at the silicon/oxide interface. The charge levels with TEOS can be as high as $1x10^{12}$ electons/cm^2. The charge at this interface can cause the formation of a channel which can connect two devices to which a connection is not desired. The original process design included a 2 μm deep trench, which was to be overfilled with TEOS to planarize the surface, so that chemical mechanical planarization would not be required. The wafers were then implanted with $7x10^{13}$ ions/cm^2 boron at 80KV. The implantation set the threshold voltage and acted as a channel stop implant. After the implant TEOS was deposited, in the original isolation scheme the TEOS would be etched back so that the desired field oxide thickness could be attained. The problem with this process is that the 2 μm wide trenches as they were filled would cause a void to form in the TEOS, as in Fig. 2

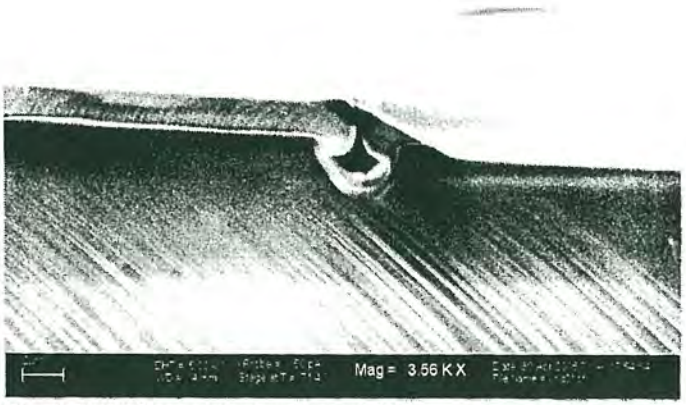

Fig. 2 Void formed during Trench fill.

The void created is shaped like a diamond, and as the TEOS was etched back planar to the surface the etch would break through into the void causing a seam formation where the trench isolation was supposed to exist. This seam made polysilicon deposition over the topography impossible. The polysilicon would fall into the void and become a discontinuous film. At this point in the process their were two choics for the formation of the trench isolation keep the 3μm thick TEOS (Fig. 2) or reduce the TEOS fill thickness and the trench depth. Both approaches were tried, however the wet etch required to create a suitable angle in the 3 μm TEOS for polysilicon coverage undercut the masking resist so that the mask defined width for the gate level is too short and the source/drains are shorted lithographically. Making the trench shallower, and the overfill less resulted in a scheme which isolated the devices, and had a small enough topography for gate coverage. The final result of this process can be seen in Fig. 3.

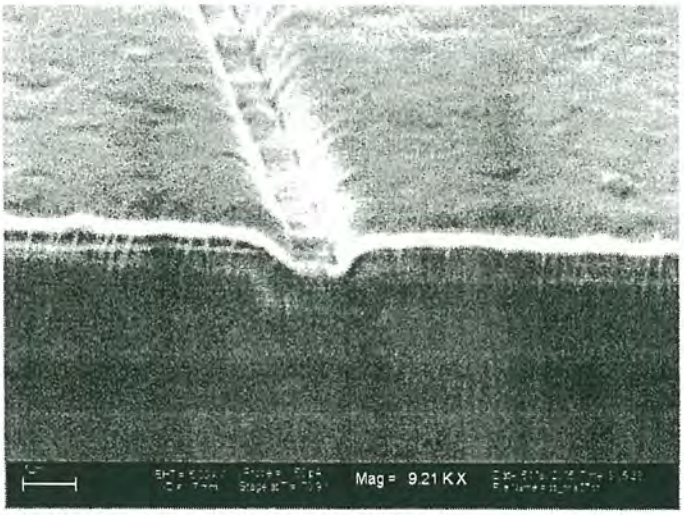

Fig. 3. Aluminum covering trench fill.

After the 1 μm trench was filled with 1 μm of TEOS, the TEOS lithographically patterned to form the active region of the device. The wafers were then lithographically patterned with the active level mask, which defined the field oxide. The field oxide was etched to silicon using HF. The resist was stripped from the wafer, and then another RCA clean was performed. The wafers were then oxidized using nitrous oxide for 1 hour at 900°C, approximately 100 angstroms of oxide were grown. Immediately, after the oxidation 2500 angstroms of polysilicon was deposited on the wafer using low pressure chemical vapor deposition. The polysilicon resistivity was measured to be beyond the range of measurement with a 4-point probe. The polysilicon was patterned lithographicaly using the optimized stepper settings. The polysilicon was etched using the Drytek Quad.. The recipe for the etch was 16 sccms of CHF_3, 8 sccms of SF_6, at 70mtorr and 185 watts for 3 minutes, on a quartz carrier. The wafer was implanted with Phosphorous at a dose of $5x10^{12}$ ions/cm^2 at 20KeV. This implant was for the formation of the low-doped source and drain region. 0.5μm of TEOS was then deposited for spacer formation. The TEOS was etched using a recipe of 70 sccms of CHF_3, 70mtorr pressure, and 185 watts. The approximate time was 9minutes and 30 seconds. This gave the spacers seen in Fig. 4.

Fig. 4. Spacers formed after anisotropic oxide etch.

After spacer formation the wafers were implanted again with Phosphorous at 20KeV with a dose of $1x10^{15}$ ions/cm^2. The implant was for source/drain formation. The dopants were activated using the rapid thermal processor, which ramped the temperature from room temperature to 950°C at 60°C/second. Then held the maximum temperature for 1 minute, and then ramped down to room temperature. The wafers were then dipped in HF, and then inserted into the CVC 601 sputter tool. Aluminum was then sputtered using a target power of 1000watts, Ar flow of 5 sccms for 35minutes. This deposited 6500 angstroms of Al with 5% Si. The aluminum was patterned using standard lithography. The aluminum was wet etched for 1 minute in aluminum etch. The wafers were sintered at 450°C for 1 hour. The final device after fabrication is shown in Fig. 5.

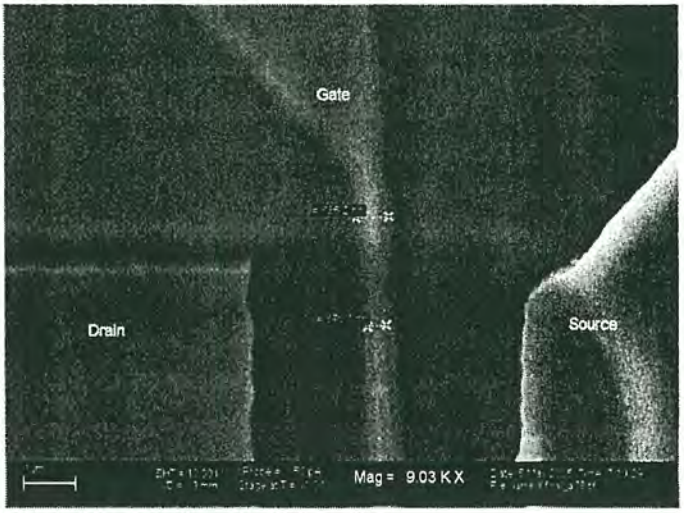

Fig. 5. Final device after fabrication.

III. Electrical Tests

The devices were test for electrical performance. The results were as follows. Fig. 6 shows the drain current as a function of drain and gate bias for a 0.37-micron transistor.

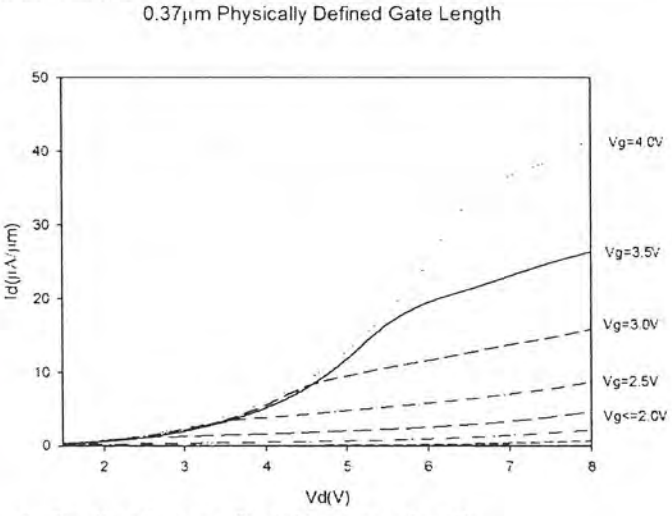

Fig. 6. Family of curves for 0.37μm gate length.

These results can be compared with that of a 0.46μm device show in Fig. 7.

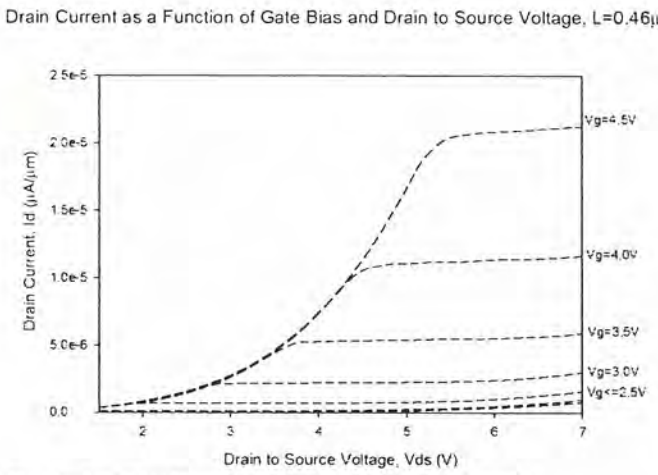

Fig. 7. Family of curves for a 0.46μm gate length.

There is a striking non-ideality in these curves, the slope of the characteristic is concave up instead of concave down. This non-ideality is indicative of a series resistance, and a non-ohmic contact. After careful analysis it is postulated that the oxide for the spacer definition process was not completely removed from the silicon. This residue oxide blocked the source/drain implant so that source and drains were low doped. This doping scenario would lead to the above curve. As the drain voltage is increased the drain becomes more and more depleted until a full depleted region forms between the channel and the drain contact, along with the low doping adding to series resistance. Also with the low doping the work function between the drain and the aluminum contact is increased leading to potential barrier formation.

The non-ohmic series resistance in Fig. 8 dominates the sub-threshold characteristics.

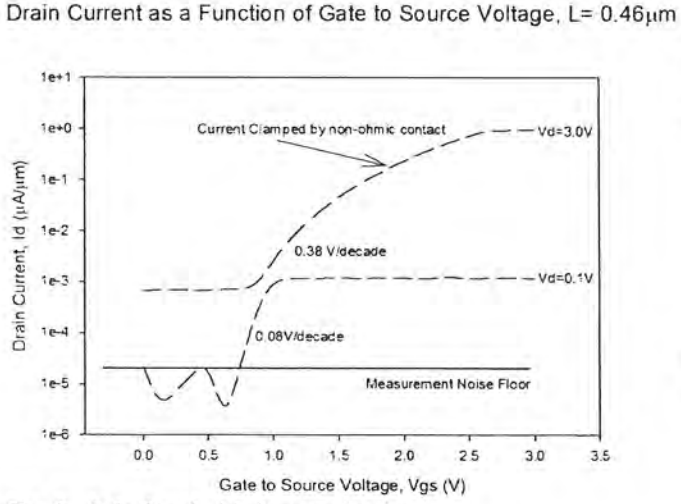

Fig. 8. Sub-threshold characterization.

The oxide etch in the Drytek is more aggressive toward the wafer edge. Near the edge of the wafer a device was found that had a more idealistic characteristic. This location of the device and its functionality leads further credence to the assertion that the oxide spacer was not cleared. The electrical results are shown in Fig. 9.

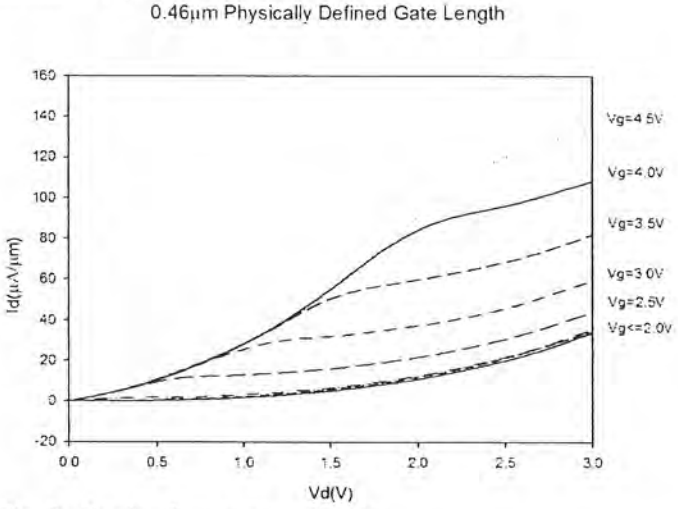

Fig. 9. Device from near wafer edge.

The devices were then tested to find out their frequency response, using a network analyzer. Active device measurements were not possible due to the unavailability of a test fixture, which provides DC blocking to the network analyzer. However, the frequency response of the pads and transmission lines were determined. The pads add an extra 5 ohms of resistance and 45pH of inductance. The frequency response of the pads is shown in Fig. 10.

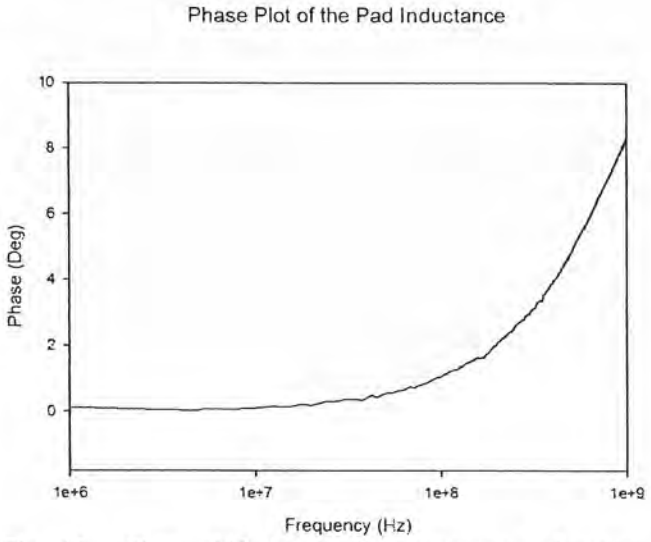

Fig. 10. Phase shift due to inductance as a function of frequency.

IV. Conclusion

A successful test layout for S-parameter analysis was demonstrated, active device measurements would have been possible with a DC blocking fixture. 0.37μm-1.0μm transistors

were fabricated with a non-ideal characteristic which was due to the source drain implant being blocked by oxide residue from the spacer formation etch.

V. ACKNOWLEDGEMENTS

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REFERENCES

[1] G. Gonzalez, **Micowave Transistor Amplifiers-Analysis and Design, 2nd Edition**, Prentice Hall, 1997.

Adam James, From Rochester, NY is graduating from the Rochester Institute of Technology in 2005 with his B.S in Microelectronic Engineering. Adam has work experience co-oping at RIT, and Silicon Laboratories, Austin TX. He will be pursuing graduate studies at the University of Illinois, at Urbana-Champaign.